More Moore:
Does It Mean Mixed-Signal Integration or Dis-Integration?

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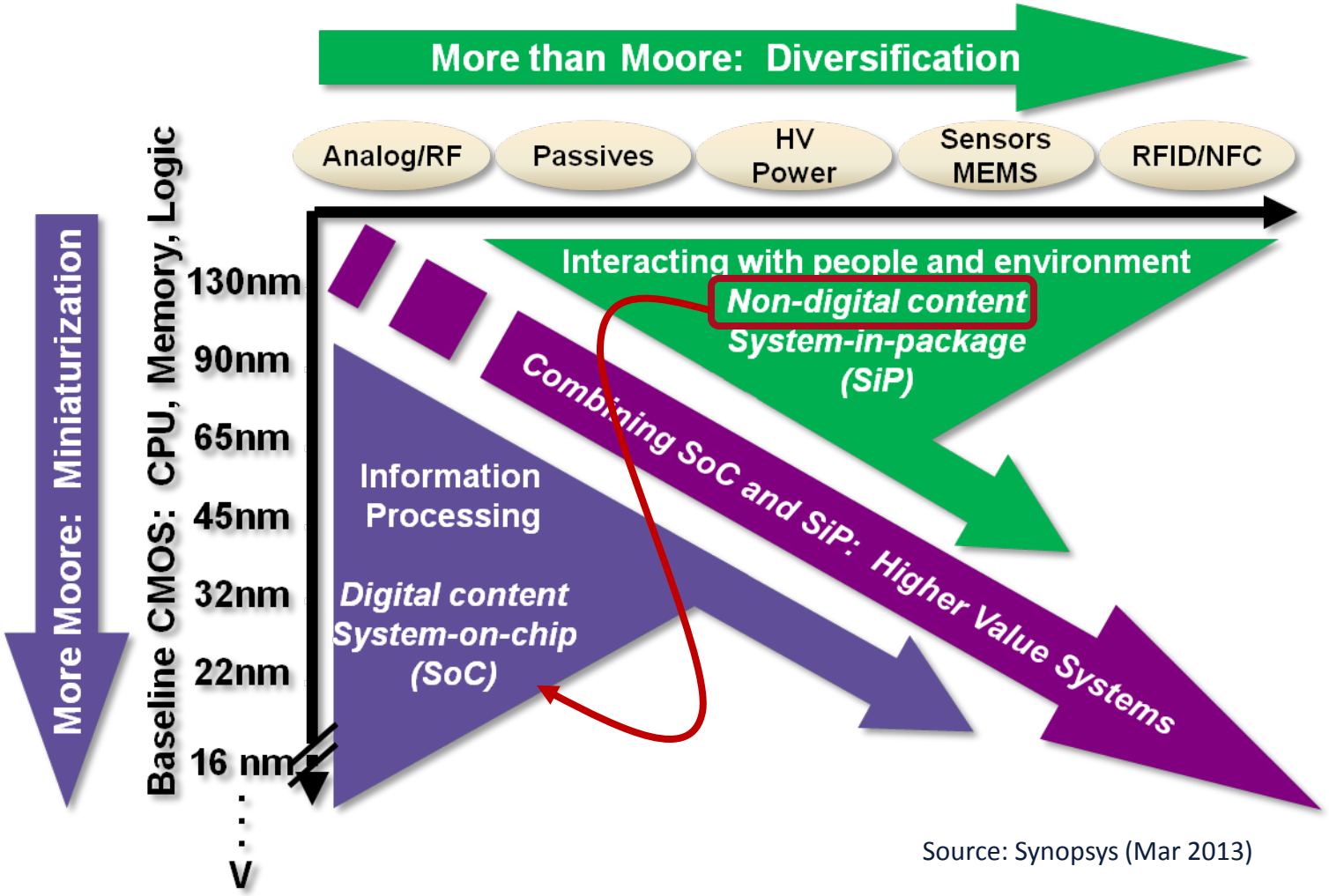
Outline

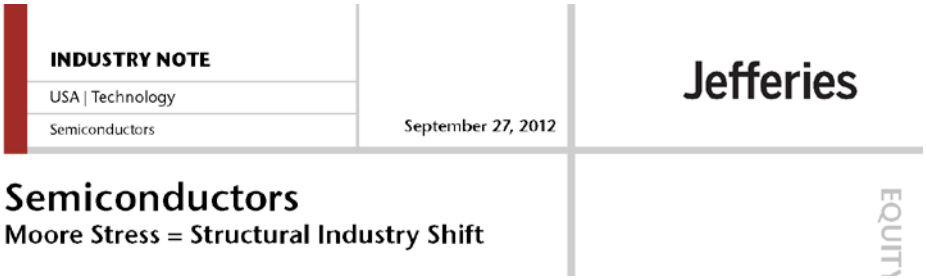
- Introduction
- Structural Shift In Semiconductor Industry
- Increasing Scaling & What It Means for AMS-RF
- Integrating AMS-RF Functionality: Why?
- Integrating AMS-RF Functionality: How?
- More Moore: What Does the Future Hold?

More Moore:
The Dominant Industry Perspective



Source: Synopsys (Mar 2013)

Structural Shift In Semi Industry


INDUSTRY NOTE
USA | Technology
Semiconductors
September 27, 2012
Jefferies
Semiconductors
Moore Stress = Structural Industry Shift
EQUITY

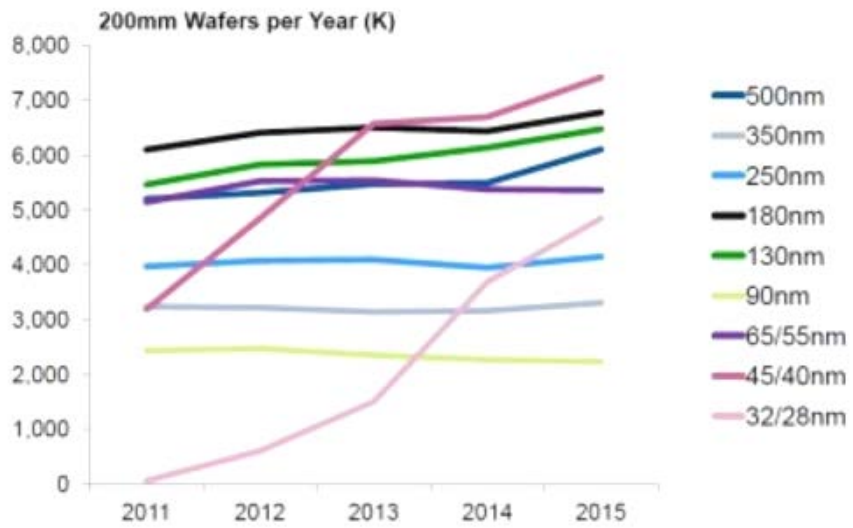
For the past 40 years, Moore's Law has accurately predicted that the number of transistors per chip doubles every two years. Equally as important as transistor density is that the cost per transistor in those chips has declined by about 30% per year. The combination of smaller, more powerful and cheaper chips every year has been the fundamental driver of the semiconductor cycle, and the foundation of innovation in electronic devices.

But something happened in 2012. Parts of the fabless industry started signaling that they were no longer seeing the normal decline in transistor cost typically associated with migrating to the most advanced manufacturing process node. Our view is that this is a critical watershed that signals a structural shift in the industry, and has many far reaching implications.

- Implications
  - Longer time between product refreshes at the leading node
  - Mixed-Signal/ Analog integrators to drive next leg of value creation to OEMs
  - Increasing capital intensity for leading-edge fab builders = near-term pain but long-term gain for survivors

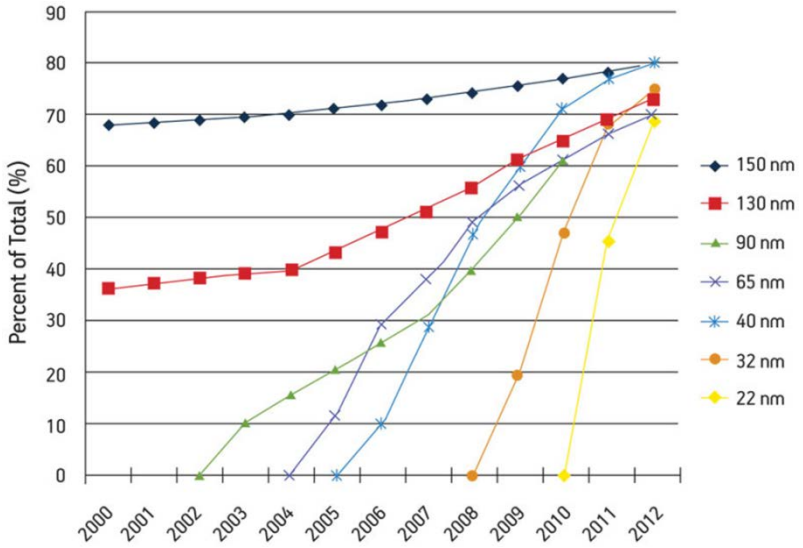
The Opportunity & The Challenge Entering 28nm

The Opportunity: Rapid Growth In Revenue at 28/20nm Nodes



Gartner, 2012

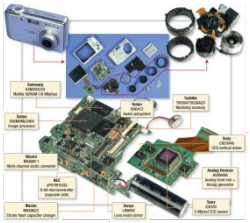
The Challenge: Rapid Increase in Mixed-Signal Content



MGC, 2011

Today, Platforms Define The Winners

And Platforms Are Rapidly Going Into Deep Nanometer

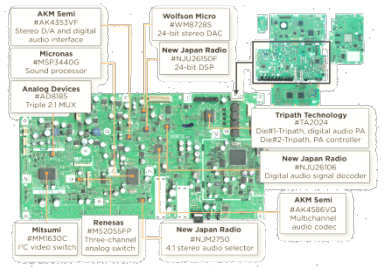


Cameras

Connectivity (Wireless/Wireline)

Application Processor

Sensors & Displays



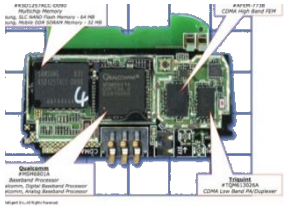
FPTV

Laptop

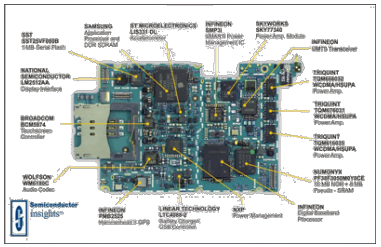
Power Management

Memory

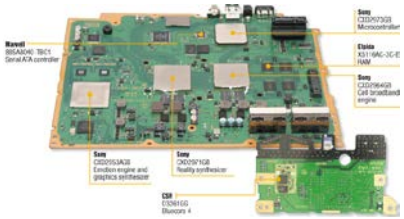
Timing Control



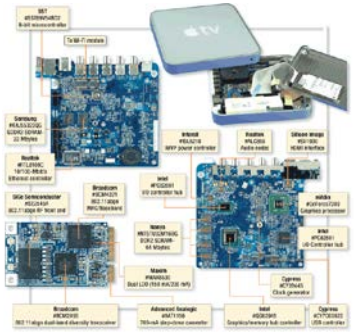
Automotive



3G/4G Mobile



Gaming



IPTV

Tablets

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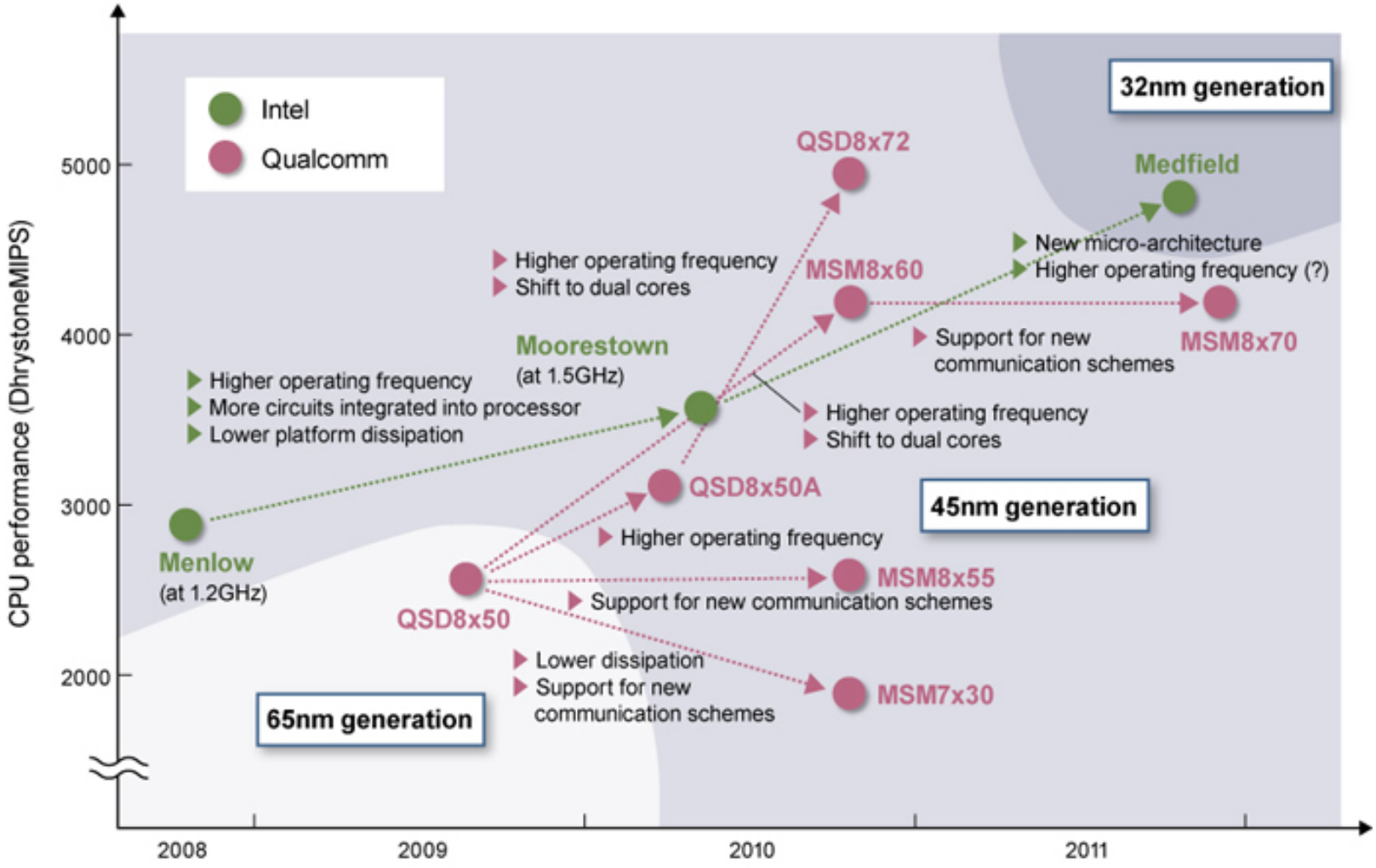
Major Platform Battles Have Begun

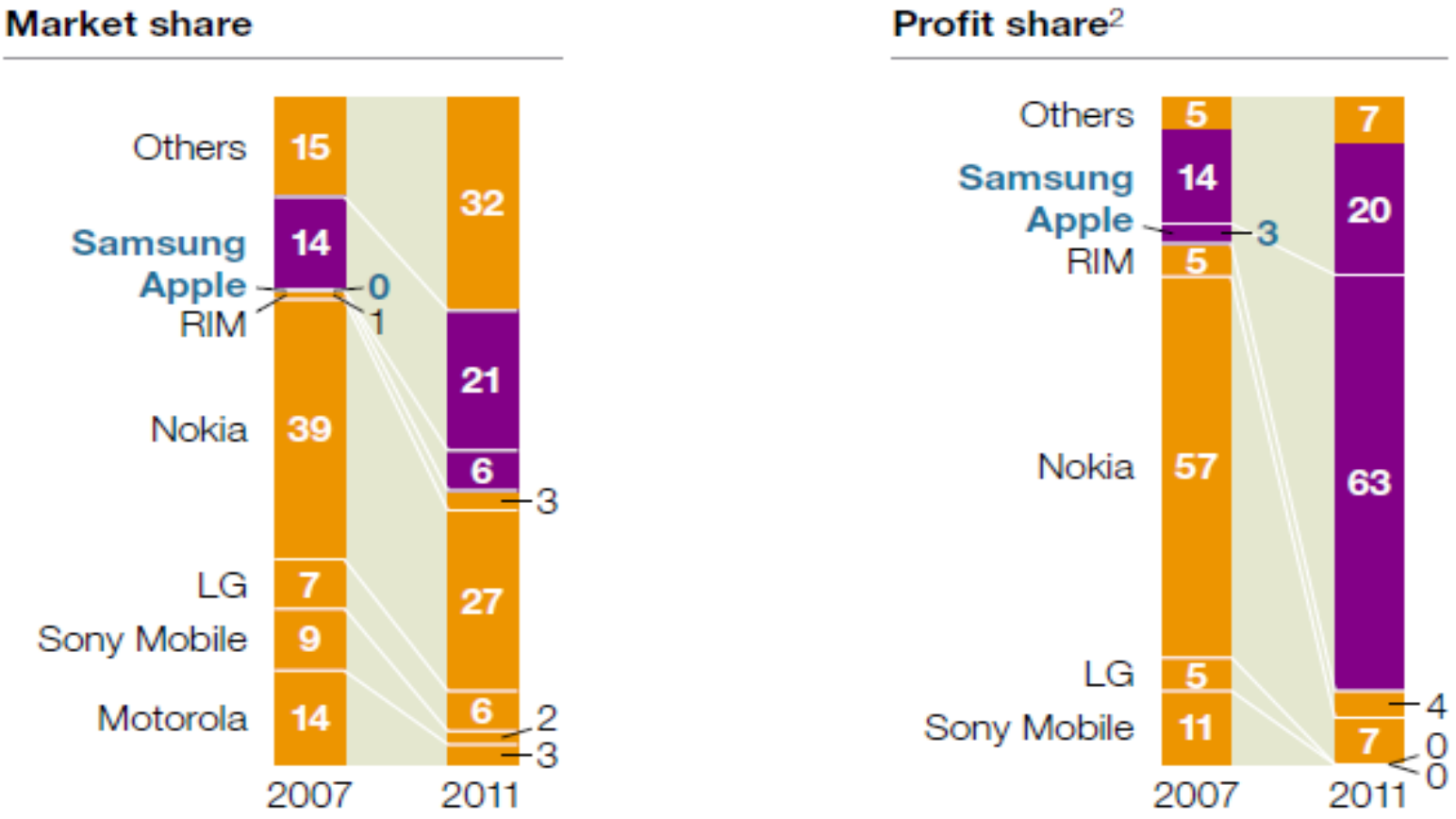


Source: Nikkei Electronics, Dec 2010

Why Increase Mixed-Signal Integration?

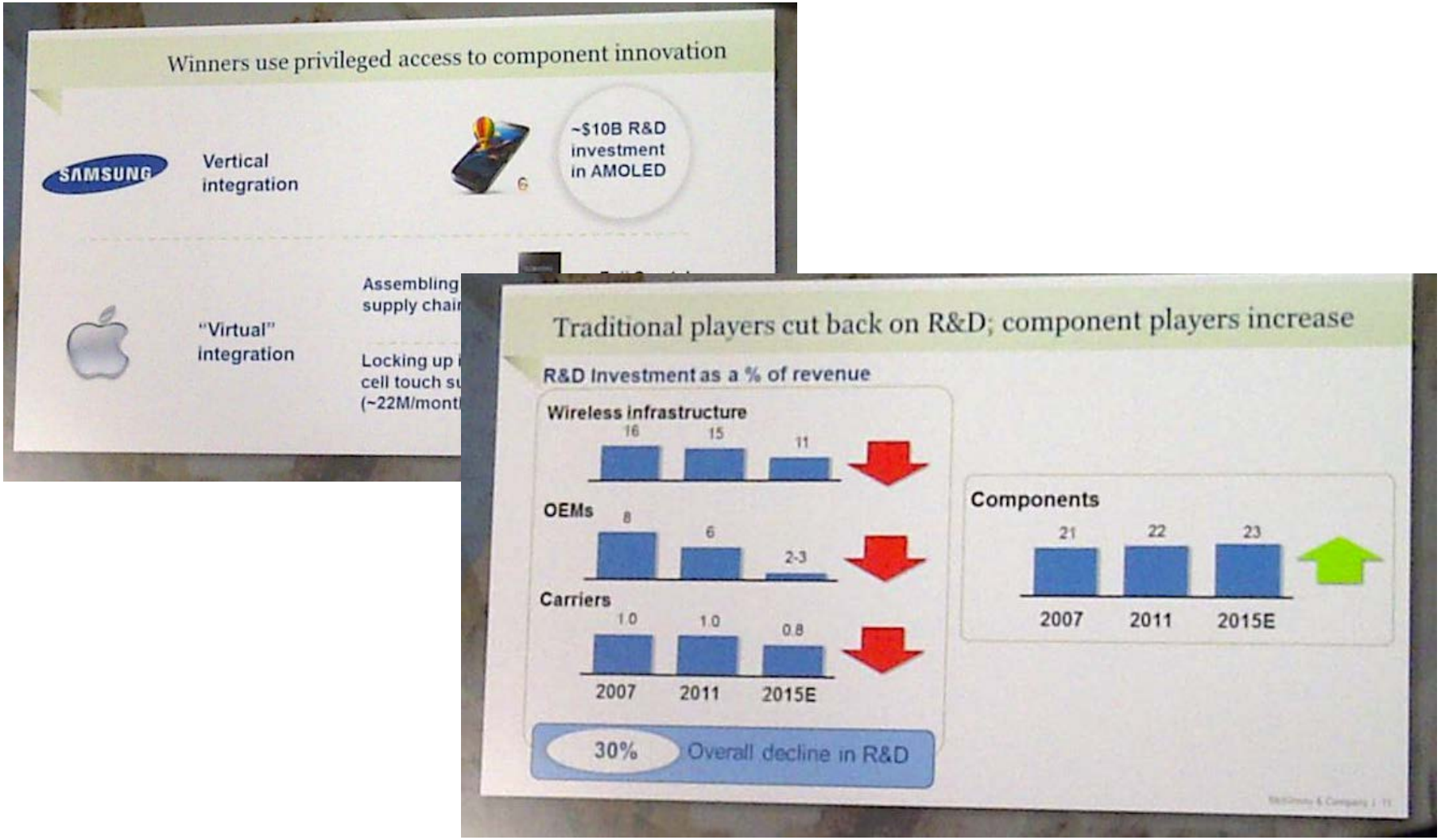
- Cost (really?)
  - Establish differentiation via Performance, Power, Cost, Features
  - Price-point of solution (not cost!)
- Platform Control
  - Control integration of key functions in a platform
  - Control of silicon bill of materials (BOM)
  - Control evolution of features on the platform
  - Software lock-in!
- Examples
  - Qualcomm, Intel, Apple, MediaTek

Platform Control Means… Profit Control



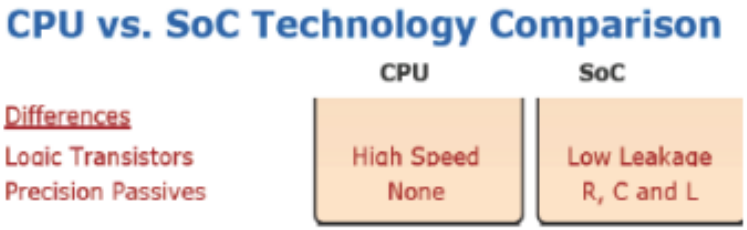
Source: McKinsey, 2012

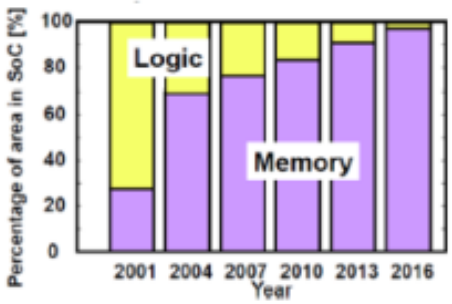
And Power Is Coming To Component Makers



Source; McKinsey, Oct. 2012

Ultra-Complex SoC: More than just multi-core CPUs…





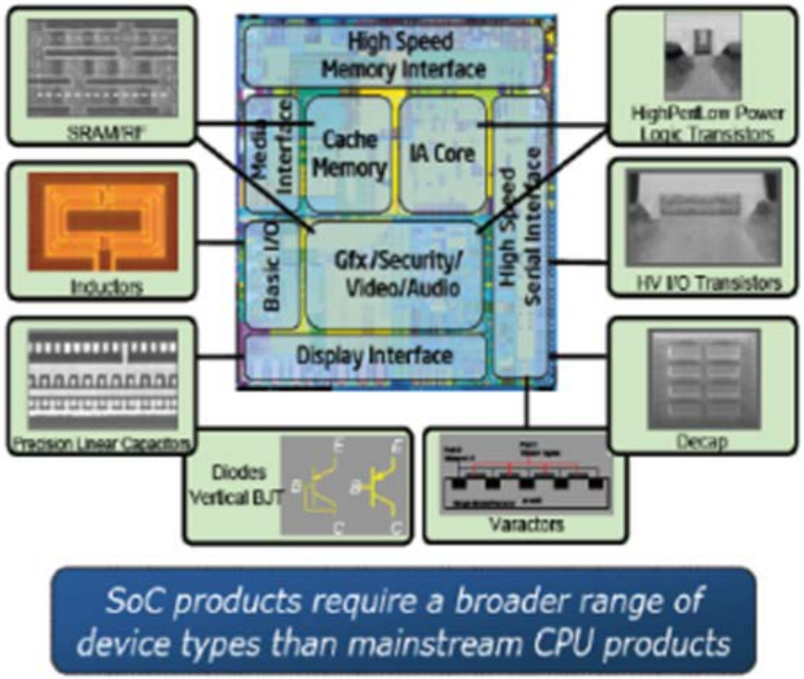
Source: Y. Nishi, S.M. Sze, EE319 Lecture Stanford 2009

- Most people say it is all about integrating digital and lots of memory (Sematech, 2009)
- Yes, but what circuitry is going to get all the data in and out?

What Comes with Increasing Integration?

- These small geometries enable extremely high-density digital circuits…
  - ..and a huge data I/O requirement (headache)
  - Digital processing is getting faster and faster, while connections between chips and system elements often remain the same and become more and more of a bottleneck.
  - The total power budget for a system also remains the same and the latest process technology does not reduce the power for many interface technologies.

SoC Building Blocks

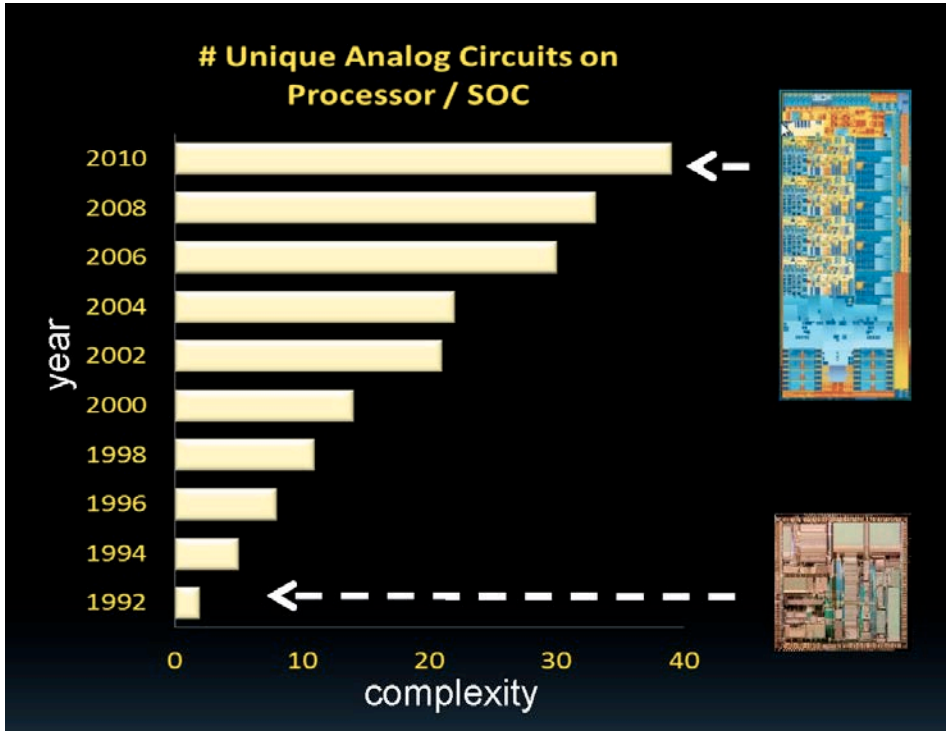


Source: Sematech 2011

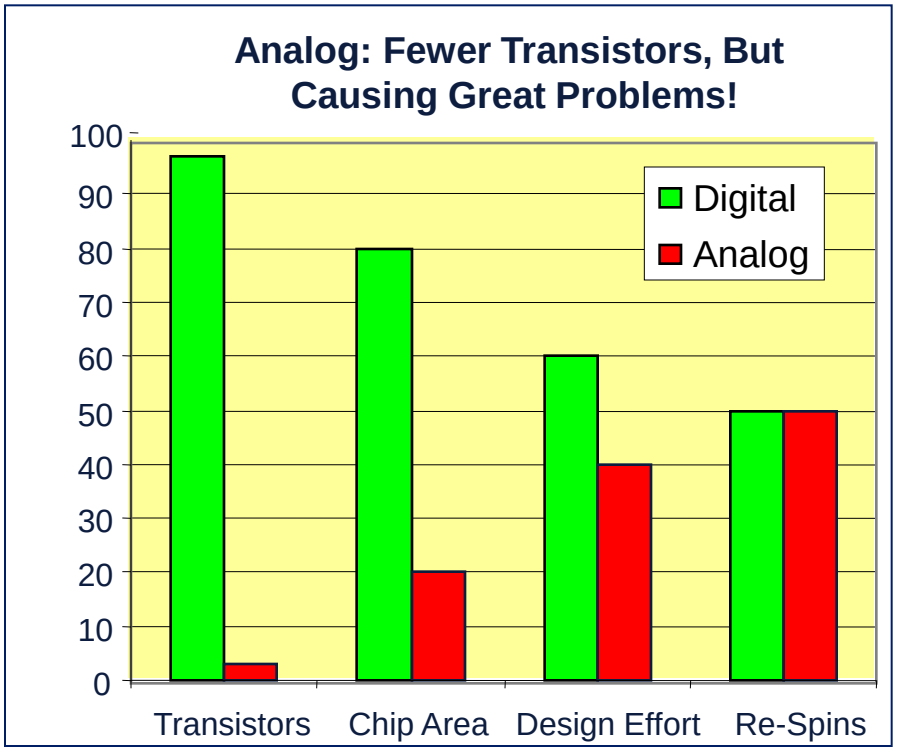
What Are These Circuits?

- What are these “huge data I/O requirements?”
- To interface with other chips on the same card, on separate cards in the system or even other systems:
  - serial interfaces using speeds of a few Gbps per lane
  - interfaces with one or multiple 10Gbps lanes (XFI, SFI, XLAUI, CAUI, and protocols all the way up to 100GbE).
  - Even higher speed interface lanes will be demanded by 12G SAS, 16G Fibre Channel and 25G Infiniband.
  - Such increased speeds mean interface technology has to become even more sophisticated.
- All these interfaces are ANALOG-rich mixed-signal circuits
- So, despite what anyone says, “More Moore” simply cannot happen without analog/mixed-signal integration!

Increasing Analog Content in CPU/SoC



Source: Intel, 2011



Source: FSA/2004

Average growth per generation

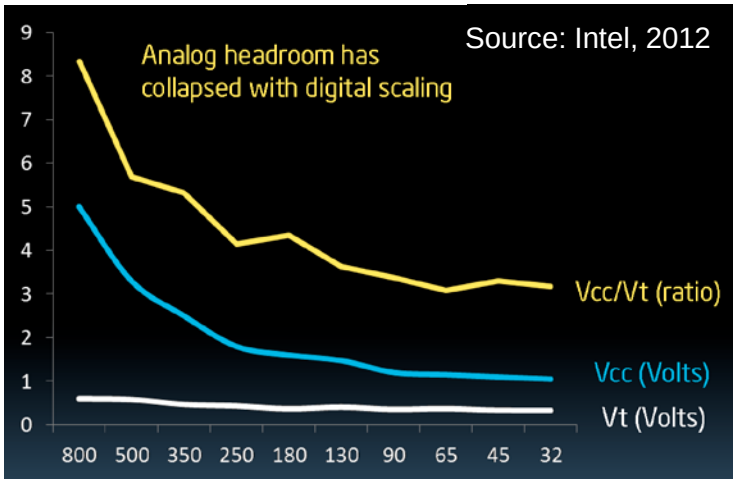
- 4 new AMS/RF circuits
- 50% improvement in performance FOM
- 2% more die area

Analog growth does not come without risk

- Increasing embedded analog content
- Faster I/O means RF circuits on-board
- Verification becomes the challenge

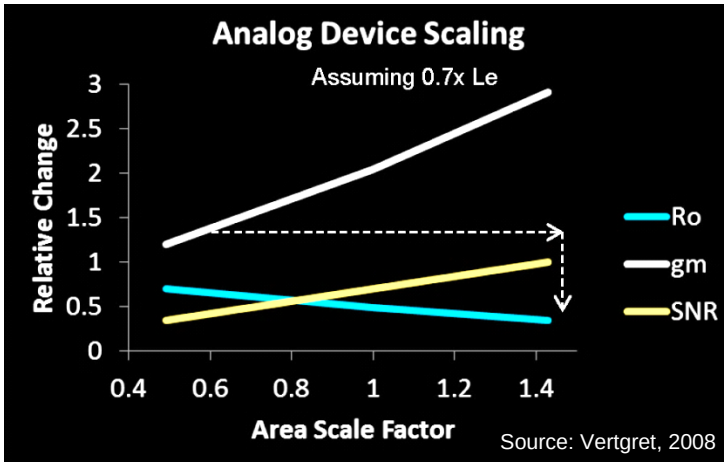
What Happens When Analog Scales

- Analog headroom collapses



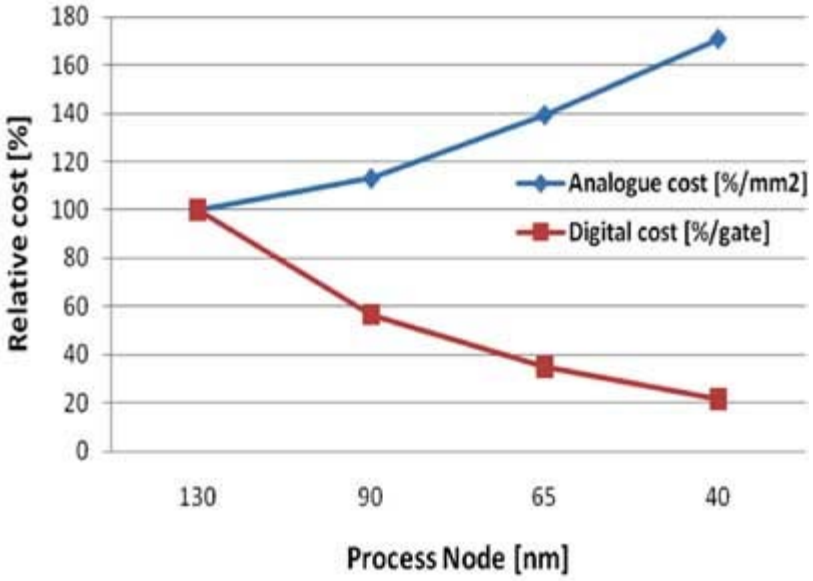
- To maintain the same performance FOM,
  - area must grow
  - current must grow

Well, OK, analog does not quite scale…



Relative Costs with Scaling: Analog v Digital

What Happens With Integration?



What Happens With Dis-Integration?

Example of power dissipation for high-speed serial transceiver

Sub-block	SoC	Disintegration
Line-side Tx (pre-emphasis)	100	100
Line-side Rx (equalization)	200	200
Chip-to-chip Tx	0	25
Chip-to-chip Rx	0	75
Total i/f power [mW]	300	400
Relative power	100%	133%

Source: A. van der Horst, "High-Speed I/O", EETimes, 10 Jan 2013

What's Needed for Ultra-Complex SoC

- Reduced cost, size, power while enjoying better performance
- Novel devices need to meet the
  - Logic
  - Static random access memory (SRAM)
  - Analog/radio-frequency(RF)
  - High-voltage
  - Input/output (I/O) requirements
- Novel circuits architectures/topologies to achieve the required performance-power-area trade-off
- New design analysis capabilities to enhance designer's ability to exploit the new technologies

Nanometer Problems Are Driving Up Platform IC Design Project Costs

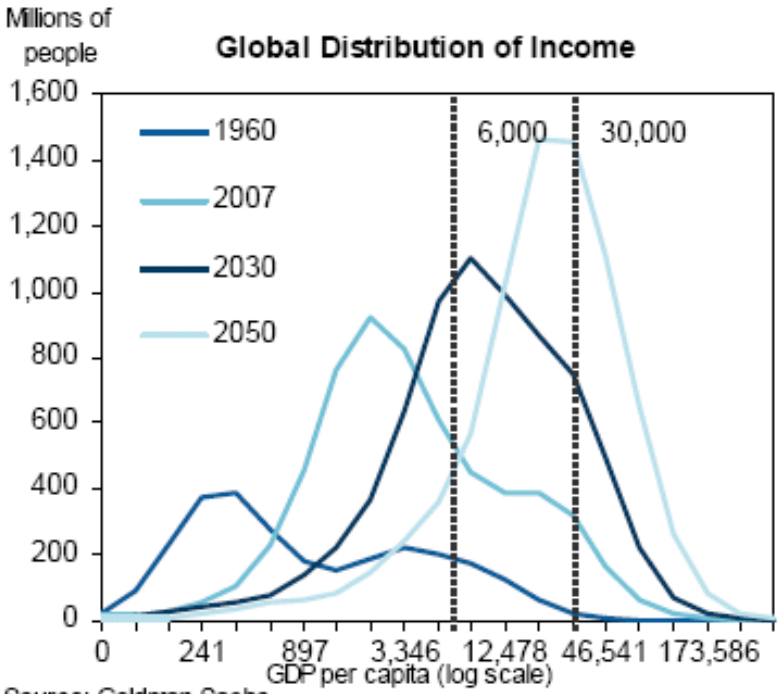
Nanometer IC Project Costs

Source: ICInsights, Xilinx (2010)

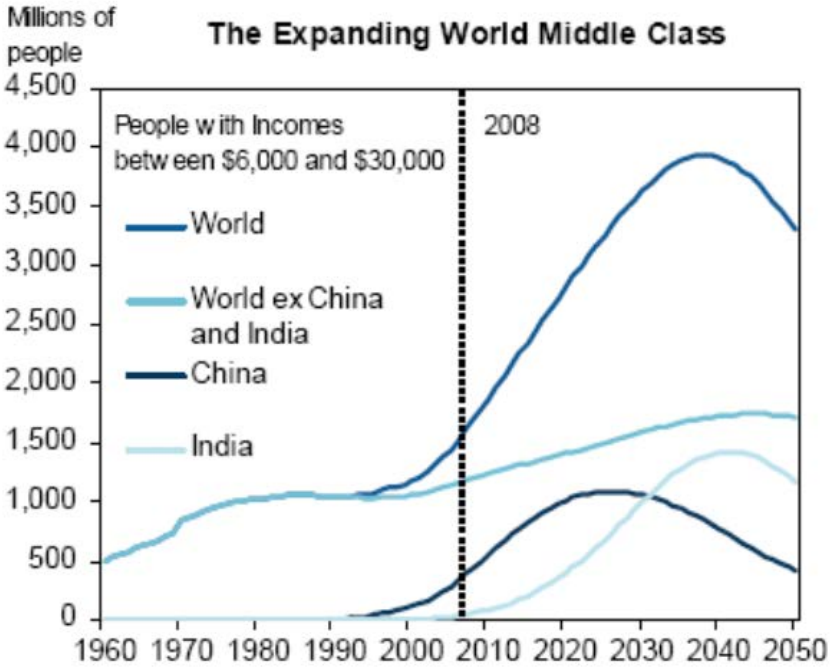
Spending Increases Target New Nanometer M/S Challenges

- Platform Complexity
  - nm RF, nm SoC, nm Storage
- Low voltage/ Low power operation
- Mixed-signal integration
- Packaging and high-frequency effects
- New 1st order physical effects
  - Device mismatch
  - Device noise
  - Detailed parasitics
  - Process variability
- Designer productivity
- Design schedules → merchant IP availability

Why Does This Matter?



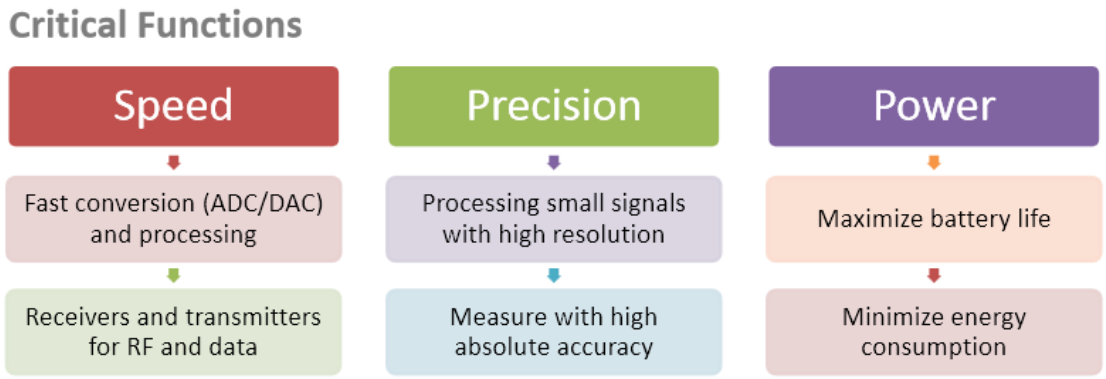
Source: Goldman Sachs



Source: Goldman Sachs

Increasing Integration

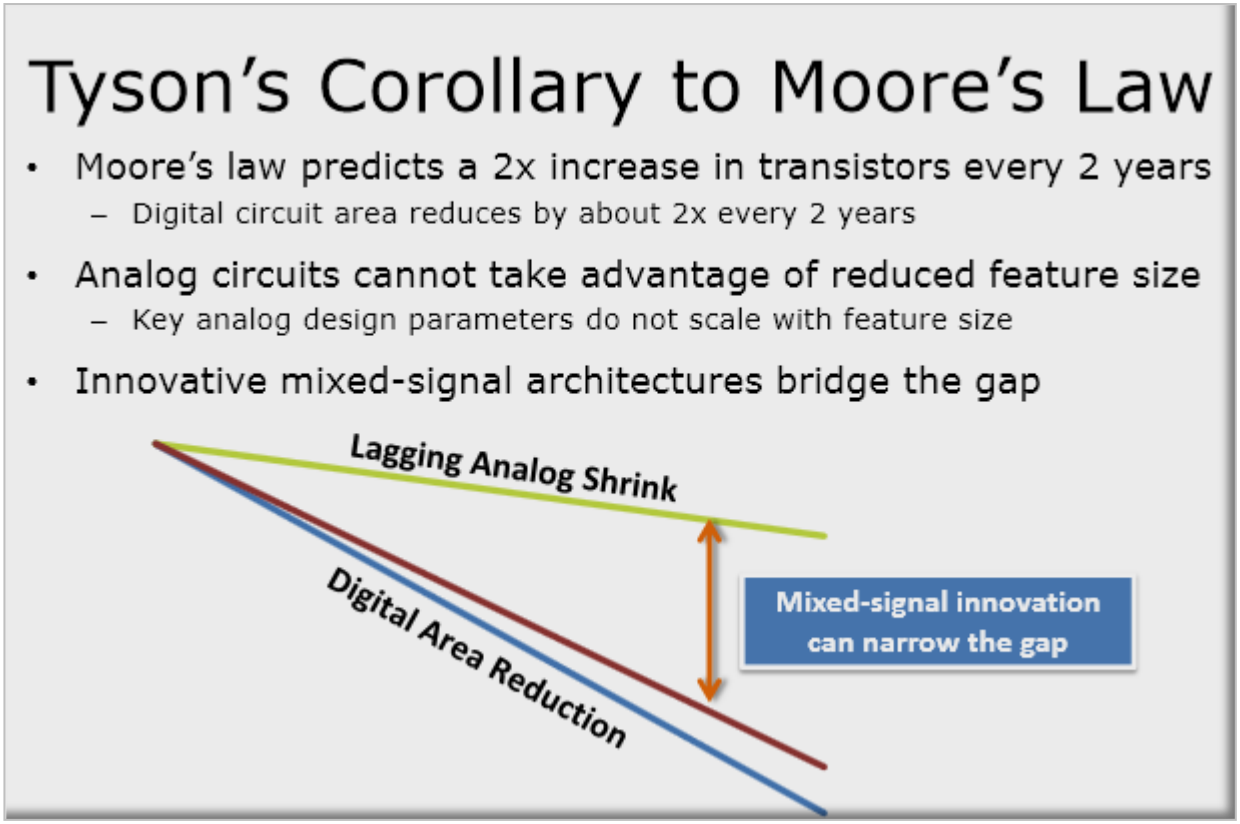
- A large, standalone analog market with very different competitive dynamics exists because integration with digital ICs causes analog performance degradation
- Yes innovation via new mixed-signal circuit architectures is enabling advanced mixed-signal devices that avoid performance compromises
- These will bring changes in three critical areas



Source: Global Semiconductor Association, Silicon Series, 2011

Analog and Moore's Law

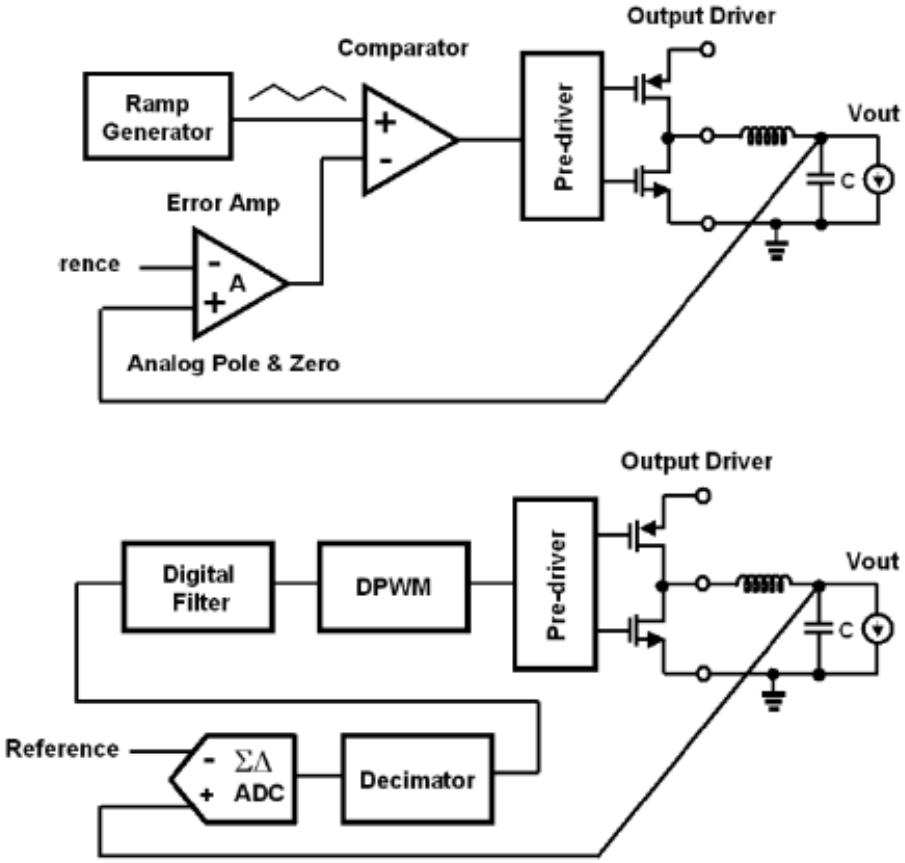
- Tyson's Corollary to Moore's Law
  - Tyson Tuttle is the CEO of Silicon Laboratories



Source: Global Semiconductor Association, Silicon Series, 2011

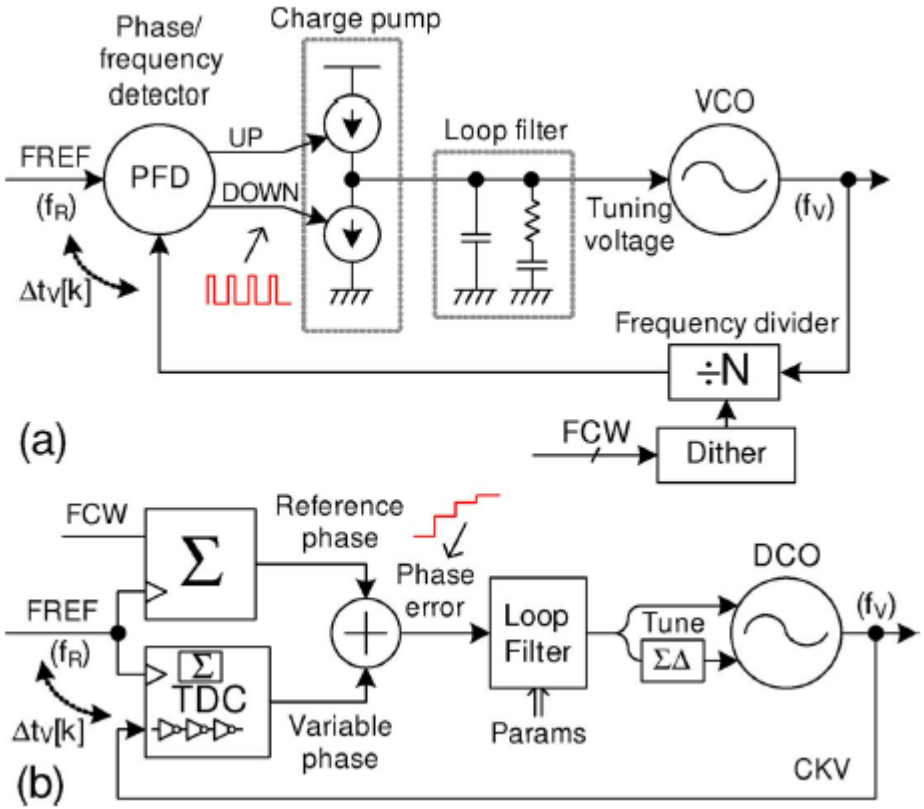
Move to Deep Nanometer brings New Circuit Architectures Innovations- I

- Example: Traditional analog vs Nanometer mixed-signal buck converter (Soenen et al. ISSCC 2010)



Move to Deep Nanometer brings New Circuit Architectures Innovations- II

- Example: Traditional analog PLL vs Nanometer mixed-signal “Digital” PLL (Staszewski et al, JSSCC Dec. 2011)



Move to Deep Nanometer brings New Circuit Architectures Innovations- II

- Example: Mismatch-robust High-Performance SC-DAC for 10G Ethernet (Daigle et al. JSSC 2012)

A 12-bit 800-MS/s Switched-Capacitor DAC with Open-Loop Output Driver and Digital Predistortion

Clayton Daigle, Alireza Dastgheib and Boris Murmann
Department of Electrical Engineering
Stanford University, Stanford, CA, USA

Abstract—A 12-bit 800-MS/s DAC implemented in 90-nm CMOS is presented. The design uses three interleaved, pipelined, switched-capacitor cores followed by an open-loop output driver. The driver is linearized using digital predistortion. Measured SFDR is greater than 58 dB for signal frequencies below 200 MHz, and greater than 53 dB for signal frequencies below 400 MHz, all with output swings as large as 2.9 V_{pp} peak-to-peak differential. Power dissipation is 103 mW when delivering a full-scale signal current of 16 mA.

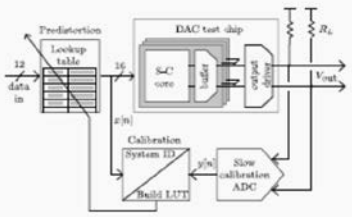


Fig. 1. Top-level block diagram of the DAC system presented in this work. The DAC uses weakly nonlinear open-loop amplifiers that are corrected using digital predistortion. Data from a slow, linear ADC is used by the calibration algorithm to build a predistortion lookup table.

I. Introduction

This paper presents a new DAC architecture intended for high-speed data transmission applications, such as 10GBASE-T. It consists of three interleaved, switched-capacitor (SC) cores followed by an open-loop output driver. The open-loop driver is weakly nonlinear and requires linearization. As shown in Fig. 1, this is achieved using a digital predistortion lookup table and a slow calibration ADC. Calibration increases the digital complexity of the DAC, but this is not prohibitive in systems where extensive digital signal processing is already required for LDPC encoding and channel precoding.

SC DACs have a number of advantages over the more prevalent current-steering architecture. The most fundamental is that SC DACs partition amplitude accuracy and timing accuracy into separate functions performed by different circuit blocks: amplitude accuracy is achieved in an SC core and depends primarily on adequate settling time and capacitor matching, while timing accuracy is achieved using a single track-and-hold switch before the final output driver. By contrast, current steering DACs perform the entire conversion at the update instant by summing together thousands of switched-current unit cells. Any mismatch among the unit cells in either current or timing will lead to distortion [1]. The switches also modulate the DAC output capacitance [2], which increases distortion for large signal swings. Furthermore, other subtleties, such as the crossing-point of switch control signals, can strongly impact dynamic performance [3], making current-steering DACs difficult to design. Finally, the layout of an N-bit pipelined SC DAC consists of a cascade of only N identical stages, whereas a current-steering DAC layout requires a grid of 2^N unit cells.

Despite these advantages, SC DACs have been absent in high-speed data transmission applications because of their inability to perform well when driving off-chip loads. SC DAC designs have instead either focused on on-chip loads [4], or they have shown that driving an off-chip load is costly in terms of power and that performance deteriorates rapidly at high frequencies [5]. The open-loop driver used in this work overcomes this significant barrier.

This paper is organized as follows: Section II describes the architecture. Section III describes the calibration and linearization scheme. Section IV presents measurement results and Section V concludes the paper.

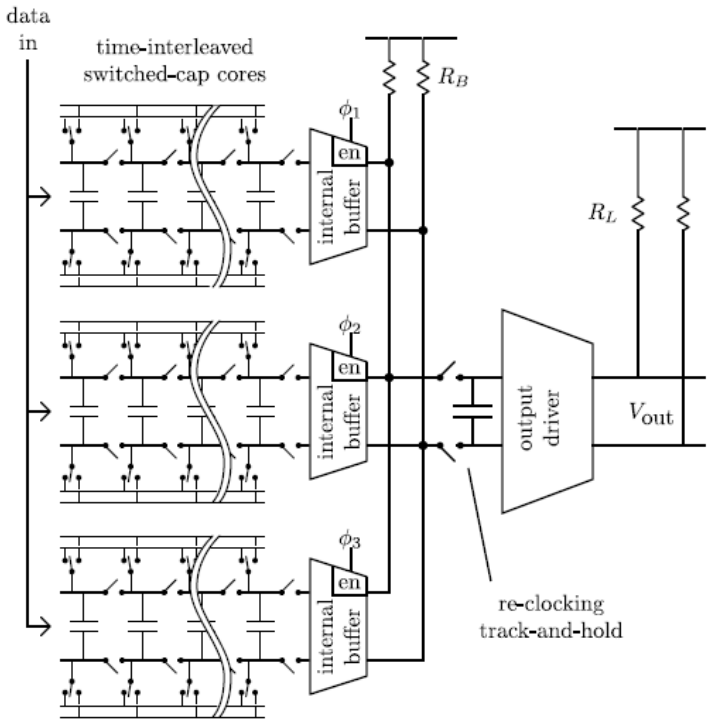
II. Proposed SC Architecture

A block diagram of the DAC is shown in Fig. 2. It consists of three time-interleaved SC cores, each with its own output buffer. These are followed by a single, shared, open-loop output driver with a track-and-hold input.

A. SC core and buffer

This design uses a pipelined, three-phase clock scheme similar to previous SC DACs [4], [5]. In order to increase throughput, three cores are time-interleaved and staggered such that one of them always has a sample ready in each of the three clock phases. Internal buffers are required at the output of each core because the cores operate through charge sharing and have very little driving capability. Without buffers, history effects in the track-and-hold circuit would cause unwanted sample-to-sample interaction.

The buffers, shown in more detail in Fig. 3, are implemented as open-loop, resistively-loaded differential pairs. Current-



FinFET's Impact on AMSRF Design

- FinFETs & Processors:
  - A way to tune for a better power/performance ratio – largely by reducing the supply voltage needed to drive the transistor.
- FinFETs & AMSRF:
  - Shift to FinFET means quantized transistor widths and need to look at new circuit topologies to work around this 'limitation.'
- Over the past 10 years, various circuit topologies have been put forward that work around the problems of width quantization
- Designers working on experimental finFET processes have reported problems such as self-heating.
  - mixed-signal designers will have to learn new layout techniques
- Finally, you also have to consider whether "*the planar transistor is really the analog designer's friend…"*

FinFETs vs Bulk FETs

- All the following make FinFETs attractive for digital and low frequency RF applications, where the performance-power trade-off is important:
  - reduced leakage
  - symmetric VTSAT
  - Excellent subthreshold slope
  - better voltage gain without degradation of noise or linearity.
- On the other hand, in high frequency applications, planar bulk MOSFETs are seen to hold the advantage due to their higher gm,max over FinFETs, whose gm is limited by series resistance.
- Understanding this trade-off is crucial for analog design.

What Are The Challenges for Design Technology?

There are three main challenges at future nodes other than complexity, which is a given challenge:

- process variation and parasitics,
- channel width and drive current choices, and
- modeling and extraction.

Any one of these three areas can become more problematic at future nodes.

K.H. Kim
EVP Foundry Business
Samsung Electronics, 2013

Mixed-Signal Design Enters The “Twilight Zone”

- Higher Precision → Simulation Noise Floor
- Increasing Device Model Complexity
- Explosion In Post-Layout Circuit Complexity: Parasitics
- Device Noise Is Now A First Order Effect
- “Corner Spread” Strikes With A Vengeance
- Increasing Complexity of nm Mixed-Signal Designs
- Reinventing Design for Low-Supply-Voltages
- Entering the World of Restricted Design Rules
- Coping With Design for Yield

Tough Problems Remain for A/MS/RF

- Parasitics: Handling complex blocks
  - Requires block level characterization of large transistor + parasitic count blocks for analysis
- Variability: devices, parasitics, layout/proximity, thermal
  - Requires more block level characterization before integration of blocks, and then multi-block/top
  - Understanding of statistical concepts in circuit simulation is a must
- Design Sensitivity
  - Requires ability to not just simulate but perform analysis to see the impact of parameter variations on circuit performance
- Noise: impact of inherent and injected noise on performance
  - Requires accurately incorporating impact of noise and nonlinearities on complex-block performance
- Mixed-Mode: Digital (calibration, control, and processing) + RF
  - Requires more (number and type) simulations to verify design functionality and performance, and lots of experiments in power supply topologies
- Capacity: Handling top-level, full-chip
  - Requires performance and functional simulations at ever greater levels of complexity including large segments of transceiver, full transceiver, digital core, pads
- Manufacturability: Catastrophic/EOL simulation, parametric yield
  - Parametric yield is a key driver for success of “RF”-rich SoC

29

Increasing Characterization Intensity Is A Fact of Life for "*nanometer analog*"

	VT Corners	Process Corner/Vars	Post-Layout	Device Noise	Device Mismatch	Combined Effects
Full Circuit						
Wireless TxRx	✓	✓	✓	✓		
High-Speed I/O	✓	✓	✓	✓		
Frequency Synthesizer	✓	✓	✓	✓		
Memory	✓	✓	✓	✓		
Complex Block						
PLL/DLL	✓✓	✓✓	✓✓	✓✓	✓	✓
ADC	✓✓	✓✓	✓✓	✓✓	✓	✓
DAC	✓✓	✓✓	✓✓	✓✓	✓	✓
Tx	✓✓	✓✓	✓✓	✓✓	✓	✓
Rx	✓✓	✓✓	✓✓	✓✓	✓	✓
Analog/RF Blocks						
VCO	✓✓✓	✓✓✓	✓✓✓	✓✓✓	✓✓✓	✓✓✓
Xtal Osc	✓✓✓	✓✓✓	✓✓✓	✓✓✓	✓✓✓	✓✓✓
PFD + CP	✓✓✓	✓✓✓	✓✓✓	✓✓✓	✓✓✓	✓✓✓
LNA + Mixer	✓✓✓	✓✓✓	✓✓✓	✓✓✓	✓✓✓	✓✓✓
Switch-Cap Filter	✓✓✓	✓✓✓	✓✓✓	✓✓✓	✓✓✓	✓✓✓

Simulations

10s

↓

100s

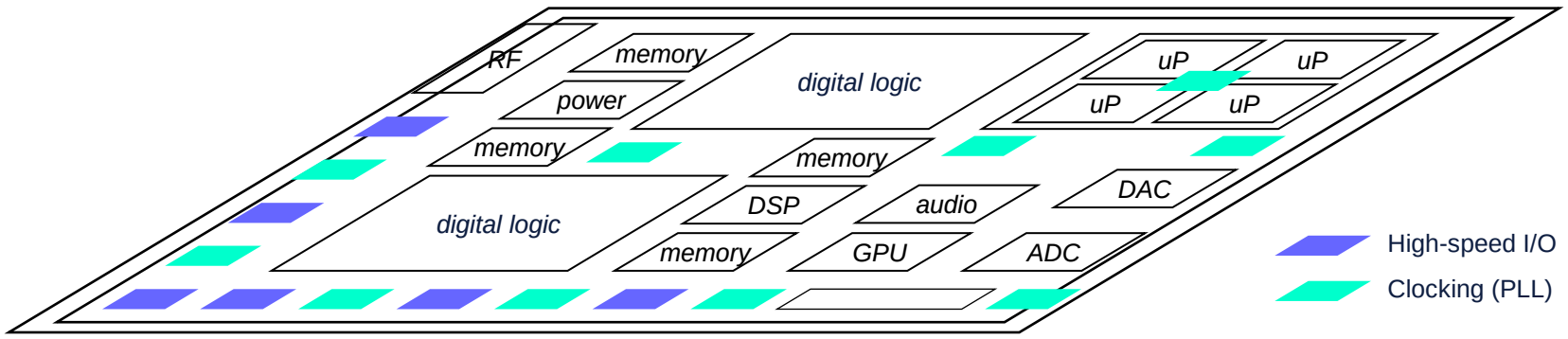
↓

1000s

✓ Selective
✓✓ Required
✓✓✓ Extensive

Ensure silicon will meet all specifications under all conditions.

Mixed-Signal SoCs



- Digital verification challenge: RTL complexity
  - *Cannot refine to transistor level (IP may not exist)*
- Analog verification challenge: performance @ required accuracy
  - *Specifications require nm SPICE accuracy (i.e., tighter than default SPICE)*
- System-level verification challenge: functional integration
  - *E.g., all digital-analog interfaces work correctly in all operating modes*

New Problems Are
Driving The Creation of a New Requirements

Traditional Markets

- SPICE
- Digital FastSPICE
- RF
- AMS

Nm Pain Points

- Circuit Complexity
- Noise & Parasitics
- RF in CMOS
- Complex Modeling

Nanometer Circuit Verification Market

Demand Drivers

- Integration (complexity, AMS, pkg)
- Frequency (clocks, data, tones)
- Power (low voltage, on-chip mgmt)

Physical Drivers

- Physical (nonlinearity, device noise)
- Layout (parasitics, design rules)
- Process (mismatch, variation, yield)

Even Tougher Problems Remain!

- Self-Interference and Co-Existence
- Impact of Substrate Noise on Mixed-Signal Complex Block and Full-Circuit performance
- Impact of Device Noise on Complex Block Performance
- Dramatically Faster Characterization in Face of Variability
- Mixed-Signal BIST

….and they are slowly but surely getting solved!

33

Outline

- ✓ Introduction
- ✓ Structural Shift In Semiconductor Industry
- ✓ Increasing Scaling & What It Means for AMS-RF
- ✓ Integrating AMS-RF Functionality: Why?
- ✓ Integrating AMS-RF Functionality: How?
- ✓ More Moore: What Does the Future Hold?

Thank You!

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